In The Specification

Rewrite the paragraph at column 4, lines 1-10 as follows.

The sources 12 of adjacent cells 10 are connected in common to another set of column lines 25 which function as virtual ground lines. Each line 25 is connected through a load device 26 to Vdd or Vx, and is also connected through a column select transistor 27 to [ground, or Vdd] Ground. The gates of all of these transistors 27 are connected via lines 28 to a ground selector 29 which receives the output lines 22 from the Y address decoder 21, along with the least significant address bit [A.sub.o] A_0 and its complement [A.sub.o.sub..sub.--] $/A_0$, and functions to activate only one of the lines 28 for a given Y address.

Rewrite the paragraph at column 4, lines 31-60 as follows.

In a write or program mode, the X address decoder 16 may function, in response to row line address signals on lines 17, and to signals from a microprocessor, to place a preselected first programming voltage Vpp (about +11 to +13V) on a selected row line Xa, including the control-gate conductor 11 of selected cell 10a. Y address decoder 21 also functions to place a second programming voltage Vp (Vpp reduced through an impedance to about +5 to +8V) on a selected drain-column line 18a and, therefore, the drain region 13 of selected cell 10a. Deselected drain-column lines 18 are floated. The selected source-column line 25 is connected to reference potential [Vdd] Ground. Deselected source-column lies 25 are charged through transistors 26 to a sufficient voltage Vx that prevents deselected cell 10b from programming. Deselected row lines are connected to a stress-reducing voltage Vy. These programming voltages create a high current (drain 13 to source 12) condition in the channel of the selected memory cell 10a, resulting in the generation near the source-channel junction of channel-hot electrons and/or avalanche-breakdown electrons (hot carriers) that are injected across the channel oxide to the floating gate 14 of the selected cell 10a. The programming time is selected to be sufficiently long to program the floating gate 14 with a negative program charge of about -2V to -6V with respect to the

channel region. The electrons injected into the floating gate 14, in turn, render the source-drain path under the floating gate 14 of the selected cell 10a nonconductive, a state which is read as a "zero" bit. Deselected cells 10 have source-drain paths under the floating gates 14 that remain conductive, and those cells 10 are read as "one" bits.

Add the following Table at column 5, after line 15.

TABLE

Connection	Read	Write	Flash Erase
Selected Row Line	3-5 V	1-13 V	0 V (All)
Deselected Row Lines	0 V	0 V	
Selected Source Line	0 V	0 V	Float or +16 V (All)
Deselected Source Lines	0 V	Float	
Selected Drain Line	1-1.5 V	5-8 V	Float or +16 V
Deselected Drain Lines	Float	Float	
P-well	0 V	0 V	+16 V
N-well	0 V	0 V	+16 V